ABSTRACT OF THE DISCLOSURE

[1050] A divider is disclosed herein. The divider includes a sequence of divide stages programmably coupled to provide a variety of divide ratios. The divider also includes one or more multiplexers to feedback the output of a divide stage to the input of a divide stage earlier in the sequence of divide stages. The divider may also include duty cycle correction circuitry and self correction logic to correct abnormal logic states. The divide stages can operate in synchronism with each other. Multiplexer functionality, self correction circuitry functionality, and divide stage functionality may be implemented in a combination latch circuit.